UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/027,856	10/19/2001	Yasumasa Kasuya	10921.102US01	1107

23552 7590 11/05/2004

MERCHANT & GOULD PC
P.O. BOX 2903
MINNEAPOLIS, MN 55402-0903

EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/027,856	KASUYA, YASUMASA	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-10 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-10 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4, 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,281,568 to Glenn et al. in view of US Patent No. 5,986,333 to Nakamura.

Regarding claim 1, Glenn et al. (figures 2-7) teach a semiconductor device comprising:

a die pad (22) including a first surface (23) and a second surface (24) opposite to the first surface, and a peripheral edge, the second surface (24) including an exposed portion and a retreated portion (a portion of the die pad formed by surfaces ([25, 26, 27]) around the exposed portion (column 5, lines 14-27). It is believed that the reference numeral for the third surface is "25" instead of "24" in column 5, line 25;

a semiconductor chip (52) mounted on the first surface (23) of the die pad (22); and

a sealing resin (51) covering the die pad (22) and the semiconductor chip (52), the resin allowing the exposed portion to be exposed and being held in contact with the retreated portion.

Glenn et al. differ from the claimed invention by not showing the die pad is formed with at least one slit that is open in the retreated portion of the second surface and in the first surface, and at least one slit is located between the peripheral edge of the die pad and the semiconductor chip, the semiconductor chip has a side facing the at least one slit and extending from a first

corner of the chip to a second comer of the chip, and the at least one slit is formed along the side of the chip and extends from a first position that is closer to the first corner of the chip to a second position that is closer to the second corner of the chip. However, Nakamura (figures 12-14) shows at least one slit (78 or 79) is located between the peripheral edge of the die pad (72) and the semiconductor chip (69), the semiconductor chip (69) has a side facing the at least one slit (78 or 79) and extending from a first corner (a portion of vertical corner of the right side chip [69]) of the chip (69) to a second comer (a portion of horizontal corner of the right side chip [69]) of the chip (69), and the at least one slit (left [78], right [78]) is formed along the side of the chip (69) and extend from a first position that is closer to the first corner of the chip (69) to a second position that is closer to the second corner of the chip (69). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Nakamura into the device taught by Glenn et al. because it absorbs thermal stress. The combined device shows the die pad is formed with at least one slit that is open in the retreated portion of the second surface and in the first surface, and at least one slit is located between the peripheral edge of the die pad and the semiconductor chip, the semiconductor chip has a side facing the at least one slit and extending from a first corner of the chip to a second comer of the chip, and the at least one slit is formed along the side of the chip and extends from a first position that is closer to the first corner of the chip to a second position that is closer to the second corner of the chip.

Regarding claim 4, the combined device shows the die pad (Nakamura; 72) is formed with a plurality of silts (Nakamura; 78 or 79) that are open in the retreated surface of the second surface (Nakamura; a bottom surface of the die pad ([72]) and in the first surface (Nakamura; a

upper surface of the die pad [72]), the plurality of slits being arranged to surround the semiconductor chip (Nakamura; 69).

Regarding claim 6, the combined device shows a terminal (Glenn et al.; a left terminal portion having surfaces [31,32,33]) electrically connected to the semiconductor chip (Glenn et al.; 52) via a wire (Glenn et al.; 54), the terminal being retained by the sealing resin so as to be partially exposed.

Regarding claim 12, Glenn et al. (figures 2-7) teach a semiconductor device comprising:

a die pad (22) including a first surface (23), a second surface (24) opposite to the first surface, and a peripheral edge, the second surface (24) including an exposed portion and a retreated portion (a portion of the die pad formed by surfaces [25, 26, 27]) around the exposed portion (column 5, lines 14-27). It is believed that the reference numeral for the third surface is "25" instead of "24" in column 5, line 25;

a semiconductor chip (52) mounted on the first surface (23) of the die pad (22), the chip having a first side and a second side adjoining the first side to define a comer between the first and second sides; and

a sealing resin (51) covering the die pad (22) and the semiconductor chip (52), the resin allowing the exposed portion to be exposed and being held in contact with the retreated portion.

Glenn et al. differ from the claimed invention by not showing the die pad is formed with a plurality of slits each of which is open in the retreated surface of the second surface and in the first surface, the slits are being located between the peripheral edge of the die-pad and the semiconductor chip, the slits face the first side and second side, respectively, of the semiconductor chip, and the plurality of slits are discontinuous with each other at the corner of

the chip. However, Nakamura (figures 12-14) shows the die pad (portion of [72]) is formed with a plurality of slits (78 or 79) each of which is open in the retreated surface of the second surface (a portion of second surface of die pad [72]) and in the first surface (a portion of first surface of die pad [72]), the slits (78 or 79) are being located between the peripheral edge of the die pad and the semiconductor chip, the slits (78) face the first side (a right portion of the chip [69]) and second side (a left portion of the chip [69]), respectively, of the semiconductor chip (69), and the plurality of slits (78) are discontinuous with each other at the corner of the chip (69). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Nakamura into the device taught by Glenn et al. because it absorbs thermal stress.

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al. in view of Nakamura, and further in view of US Patent No. 5,410,182 to Kurafuchi et al.

Regarding claim 2, the disclosures of Glenn et al. and Nakamura are discussed as applied to claims 1, 4 and 6 above.

Glenn et al. and Nakamura differ from the claimed invention by not showing the retreated portion is defined by a retreated surface and a side surface, which adjoins the exposed portion and forms an acute angle together with the retreated surface. However, Kurafuchi et al. teach the die pad (11), which has an acute angle (column 4, lines 12-15). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Kurafuchi et al. into the device taught by Glenn et al. and Nakamura because it improves the adhesion between the die pad and the sealing resin. The combined device shows the

retreated portion is defined by a retreated surface and a side surface which adjoins the exposed portion and forms an acute angle together with the retreated surface.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al. in view of Nakamura, and further in view of US Patent No. 6,566,168 to Gang.

Regarding claim 5, the disclosures of Glenn et al. and Nakamura are discussed as applied to claims 1, 4 and 6 above.

Glenn et al. and Nakamura differ from the claimed invention by not showing the die pad being electrically connected to the semiconductor chip via a wire. However, Gang (figure 7) teaches the die pad (50) being electrically connected to the semiconductor chip (44) via a wire (42). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Gang into the device taught by Glenn et al. and Nakamura because it provides interconnection between the chip and the die pad.

5. Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al. in view of US Patent No. 6,566,168 to Gang, and further in view of Nakamura.

Regarding claim 7, Glenn et al. (figures 2-7) teach a semiconductor device comprising:

a semiconductor chip (52);

a die pad (22) including an upper surface on which the semiconductor chip (52) is mounted and a lower surface opposite to the first surface;

a plurality of leads (30) spaced form the die pad via a clearance and electrically connected to the semiconductor chip (52) via wires (54);

and a sealing resin (51) enclosing the semiconductor chip (52) in a manner such that the lower surface of the die pad (22) is exposed;

wherein the die pad (22) includes a thin-walled portion formed by removing a part of the lower surface (a portion of the die pad formed by surface (25, 26, 271) along a peripheral edge of the die pad (22).

Glenn et al. differ from the claimed invention by not showing the die pad being electrically connected to the semiconductor chip via a wire. However, Gang (figure 7) teaches the die pad (50) being electrically connected to the semiconductor chip (44) via a wire (42). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Gang into the device taught by Glenn et al. because it provides interconnection between the chip and the die pad. The combined device shows the die pad being electrically connected to the semiconductor chip via a wire.

Glenn et al. and Gang differ from the claimed invention by not showing the die pad formed with at least one slit extending through the thin-walled portion, and at least one slit is located inwardly from the clearance and between the peripheral edge of the die pad and the semiconductor chip, the semiconductor chip has a side facing the at least one slit and extending from a first corner of the chip to a second comer of the chip, and the at least one slit is formed along the side of the chip and extends from a first position that is closer to the first corner of the chip to a second position that is closer to the second corner of the chip. However, Nakamura (figures 12-14) shows the die pad (72) formed with at least one slit (78 or 79) extending through the thin-walled portion, and at least one slit (78 or 79) is located inwardly from the clearance (a portion of the slit [78 or 79] is located in the clearance area between the die pad [72] and the lead

[75]) and between the peripheral edge of the die pad (72) and the semiconductor chip (69), the semiconductor chip (69) has a side facing the at least one slit (78 or 79) and extending from a first corner (a portion of vertical corner of the right side chip [69]) of the chip (69) to a second comer (a portion of horizontal corner of the right side chip [69]) of the chip (69), and the at least one slit (left [78], right [78]) is formed along the side of the chip (69) and extend from a first position that is closer to the first corner of the chip (69) to a second position that is closer to the second corner of the chip (69). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Nakamura into the device taught by Glenn et al. and Gang because it absorbs thermal stress. The combined device shows the die pad formed with at least one slit extending through the thin- walled portion, and at least one slit is located inwardly from the clearance and between the peripheral edge of the die pad and the semiconductor chip, the semiconductor chip has a side facing the at least one slit and extending from a first corner of the chip to a second comer of the chip, and the at least one slit is formed along the side of the chip and extends from a first position that is closer to the first corner of the chip to a second position that is closer to the second corner of the chip.

Regarding claim 8, the combined device shows the sealing resin (Gle1m; 51) extends under the thin-walled portion so as not to expose an opening of the slit.

Regarding claim 9, the combined device shows the at least one slit (Nakamura; 78 or 79) extends along at least one side surface of the semiconductor chip (Nakamura; 69) around the semiconductor chip.

Regarding claim 10, the combined device shows the wire (Gang; 42) is connected at one end thereof to the semiconductor chip (Gang; 44) and connected at another end thereof to the die pad (Gang; 50) at a portion between a peripheral edge of the die pad and the at least one slit.

Response to Arguments

Applicant's arguments filed 09/10/04 have been fully considered but they are not persuasive.

It is argued, in page 6 of the remarks, that Glenn et al. and Nakamura do not teach or suggest the slits extend from a first position that is closer to the first corner of the chip to a second position that is closer to the second corner of the chip. This argument is not convincing because the combined device (Glenn et al. and Nakamura) shows the slits extend from a first position that is closer to the first corner of the chip to a second position that is closer to the second corner of the chip for the reasons that are discussed above.

It is argued, in page 7 of the remarks, that Glenn et al., Gang and Nakamura do not teach or suggest the slits extend from a first position that is closer to the first corner of the chip to a second position that is closer to the second corner of the chip. This argument is not convincing because the combined device (Glenn et al., Gang and Nakamura) shows the slits extend from a first position that is closer to the first corner of the chip to a second position that is closer to the second corner of the chip for the reasons that are discussed above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
October 28, 2004

Sara Crane
Primary Examiner